

CLAIMS

What is claimed is:

1 1. A register renaming system for out-of-order execution of a set of  
2 reduced instruction set computer instructions having addressable  
3 source and destination register fields, adapted for use in a  
4 computer having an instruction execution unit with a register file  
5 accessed by read address ports and for storing instruction  
6 operands, the system comprising:

7 (a) data dependance check means for determining data  
8 dependencies between the instructions;

9 (b) tag assignment means for generating one of more  
10 tags to specify the location of operands, based on said data  
11 dependencies determined by said data dependance check means;  
12 and

13 (c) register file port means for selecting said tags  
14 generated by said tag assignment means and passing said tags onto  
15 the read address ports of the register file for storing execution  
16 results.

1 2. The system of claim 1, wherein said data dependance check means  
2 determines said data dependencies by comparing the addresses of  
3 the source register field of each instruction to the addresses of the  
4 destination register fields.

1 3. The system of claim 1, further comprising temporary storage means  
2 for temporarily storing out-of-order execution results, wherein said  
3 out-of-order execution results are passed to the register files in  
4 order after execution of the set of instructions is completed.

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1 4. A register renaming method for performing out-of-order execution  
2 of a set of reduced instruction set computer instructions having  
3 addressable source and destination register fields, adapted for use  
4 in a computer having an instruction execution unit with a register  
5 file accessed by read address ports and for storing instruction  
6 operands, the method comprising the steps of:

7 (1) determining data dependencies between the  
8 instructions;

9 (2) performing at least one of in-order and out-of-order  
10 issuing of two or more of the instructions in the instruction  
11 execution unit;

12 (3) storing, temporarily, any out-of-order results in  
13 temporary storage means;

14 (4) generating one or more tags to specify the location  
15 of said out-of-order results based on said data dependencies;

16 (5) selecting appropriate ones of said tags corresponding  
17 to the issued instruction; and

18 (6) passing said selected tags onto the read address ports  
19 of the register file for one of:

20 (i) accessing said out-of-order results; and

21 (ii) storing execution results.

1 5. The method of claim 4, wherein said determining step further  
2 comprises the step of comparing the addresses of the source  
3 register field of each instruction to the addresses of the destination  
4 register fields.

1 6. The method of claim 4, further comprising the step of storing  
2 in-order results in the register file and the temporary storage  
3 means.

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1 7. The method of claim 4, further comprising the step of passing said  
2 out-of-order results to the register files in-order after execution of  
3 the set of instructions is completed.

1 8. A method for issuing instructions in a superscalar reduced  
2 instruction set computer having an instruction issuer system  
3 capable of issuing a plurality of instructions in a single cycle, the  
4 system having more than one register file sets, the method  
5 comprising the steps of:

6 prioritizing instructions to be issued according to the  
7 number of different register file sets furnishing operands to the  
8 instruction; and

9 issuing instructions according to said prioritizing step.

1 9. The method according to claim 8, wherein said prioritizing step  
2 assigns a higher priority to those instructions having operands  
3 furnished from the greater number of register file sets.

1 10. An instruction issuer system in a superscalar reduced instruction  
2 set computer, the system capable of issuing a plurality of  
3 instructions in a single cycle, the system having more than one set  
4 of register files, the system comprising:

5 first means for prioritizing instructions to be issued  
6 according to the number of different register files furnishing  
7 operands to the instruction; and

8 second means, responsive to said first means, for  
9 issuing instructions according to said priority.

1 11. The system according to claim 10, wherein said first means further  
2 assigns a higher priority to those instructions having operands  
3 furnished from the greater number of register files.

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